WHAT IS CLAIMED IS:

1. A hard-macro arranged on a semiconductor chip for constituting a part of a semiconductor integrated circuit, including at least one wire passing therethrough, wherein said wire is formed in said hard-macro before said hard-macro is arranged on said semiconductor chip, and said wire starts a first outer edge of said hard-macro and terminates at a second outer edge of said hard-macro intersecting with said first outer edge.

2. The hard-macro as set forth in claim 1, wherein said first and second outer edges are perpendicular to each other.

3. The hard-macro as set forth in claim 1, wherein said first and second outer edges are adjacent to each other.

4. The hard-macro as set forth in claim 1, wherein said wire is L-shaped.

5. The hard-macro as set forth in claim 1, wherein said wire is linear.

6. The hard-macro as set forth in claim 1, wherein said hard-macro has a cut-out including one of corners of said hard-macro, and said wire extends along said cut-out between said first and second outer edges.

7. The hard-macro as set forth in claim 6, wherein said cut-out is rectangular, and said wire is L-shaped.

8. The hard-macro as set forth in claim 1, further including a repeater inserted in said wire.

9. The hard-macro as set forth in claim 1, wherein said hard-macro includes a plurality of wires passing therethrough.

10. The hard-macro as set forth in claim 9, wherein said wires are equally spaced away from adjacent ones.

11. The hard-macro as set forth in claim 9, wherein at least one of said wires includes a repeater inserted therein.

12. The hard-macro as set forth in claim 1, wherein said wire is divided into a plurality of portions each of which is arranged in each of a plurality of hierarchies of said hard-macro.

13. The hard-macro as set forth in claim 1, wherein said hard-macro is a random access memory (RAM).

14. The hard-macro as set forth in claim 1, wherein said hard-macro is a phase-locked loop (PLL) circuit.

15. A semiconductor integrated circuit including a hard-macro arranged on a semiconductor chip for constituting a part of said semiconductor integrated circuit, including at least one wire passing therethrough, wherein said wire is formed in said hard-macro before said hard-macro is arranged on said semiconductor chip, and said wire starts a first outer edge of said hard-macro and terminates at a second outer edge of said hard-macro intersecting with said first outer edge.

16. The semiconductor integrated circuit as set forth in claim 15, wherein said semiconductor integrated circuit is a cell base integrated circuit (CBIC).

17. A floor-planner including a device for analyzing a floor-plan of a semiconductor integrated circuit including a hard-macro arranged on a semiconductor chip for constituting a part of said semiconductor integrated circuit which hard-macro includes at least one wire passing therethrough, wherein said wire is formed in said hard-macro before said hard-macro is arranged on said semiconductor chip, and said wire starts a first outer edge of said hard-macro and terminates at a second outer edge of said hard-macro intersecting with said first outer edge.

18. The floor-plan as set forth in claim 17, wherein said device analyzes a route of said wire.

19. A program for causing a computer to analyze a floor-plan of a semiconductor integrated circuit, wherein said semiconductor integrated circuit includes a hard-macro arranged on a semiconductor chip for constituting a part of said semiconductor integrated circuit which hard-macro includes at least one wire passing therethrough, wherein said wire is formed in said hard-macro before said hard-macro is arranged on said semiconductor chip, and said wire starts a first outer edge of said hard-macro and terminates at a second outer edge of said hard-macro intersecting with said first outer edge.

20. The program as set forth in claim 19, wherein said computer further analyzes a route of said wire.